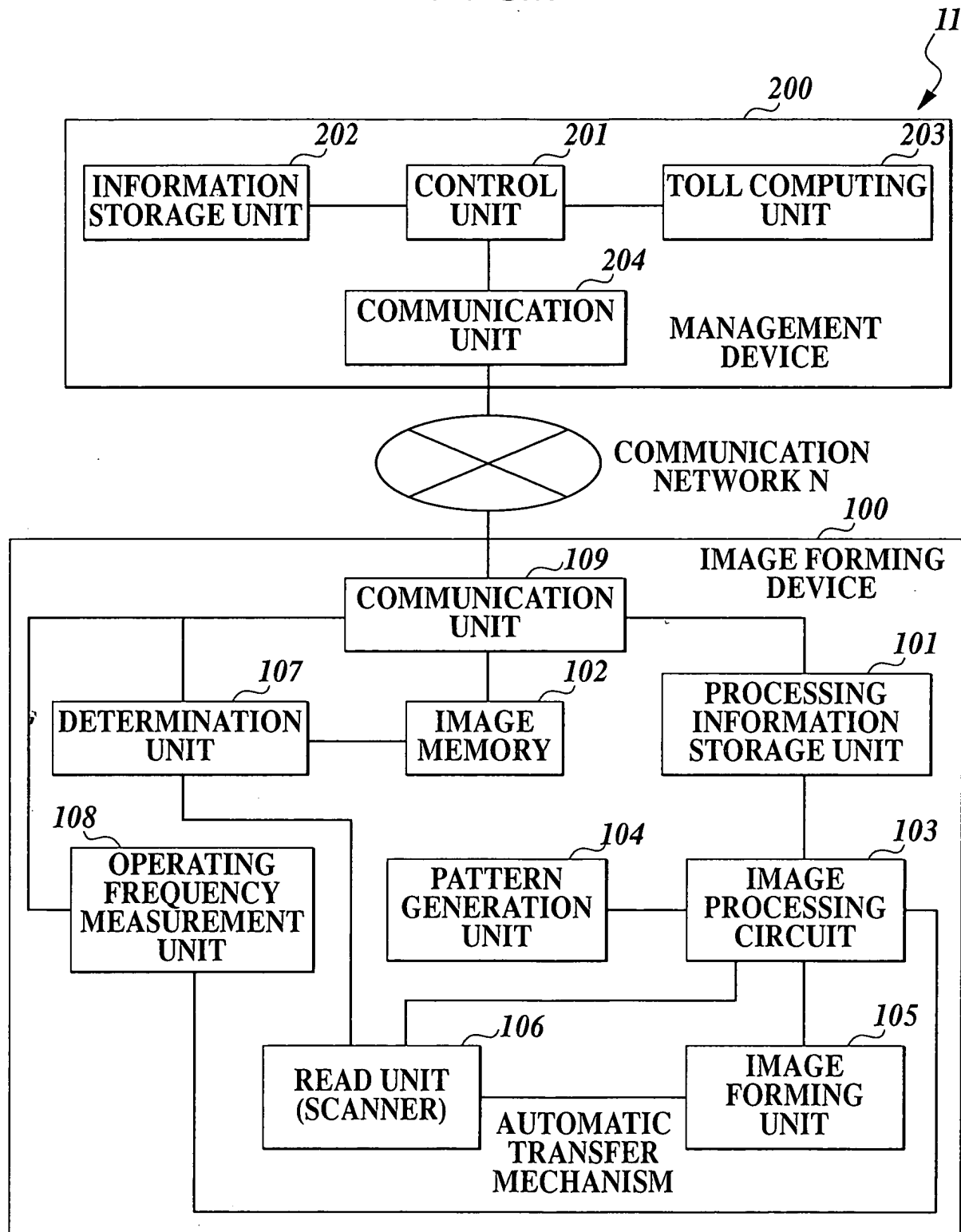


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**FIG.1**



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**FIG.2**

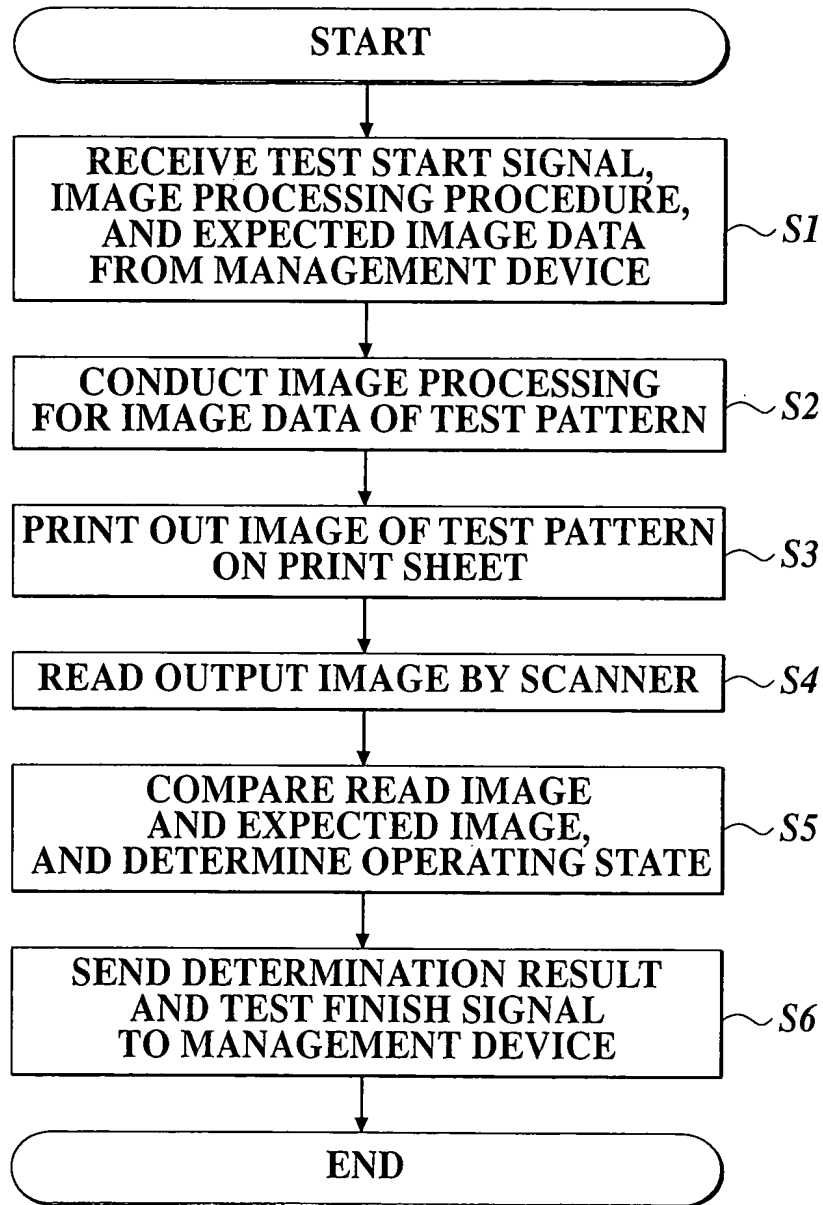


FIG.3A

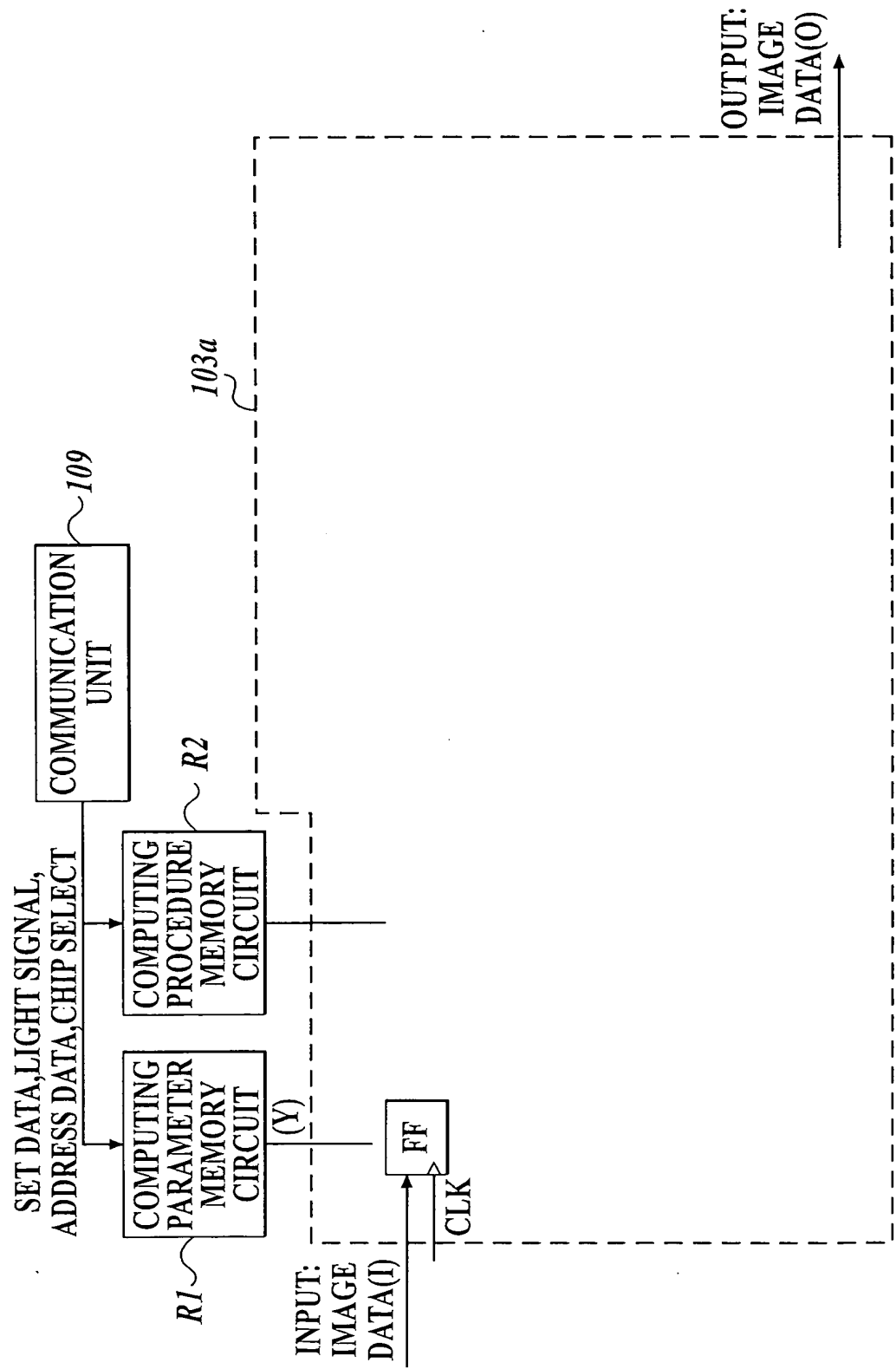


FIG.3B

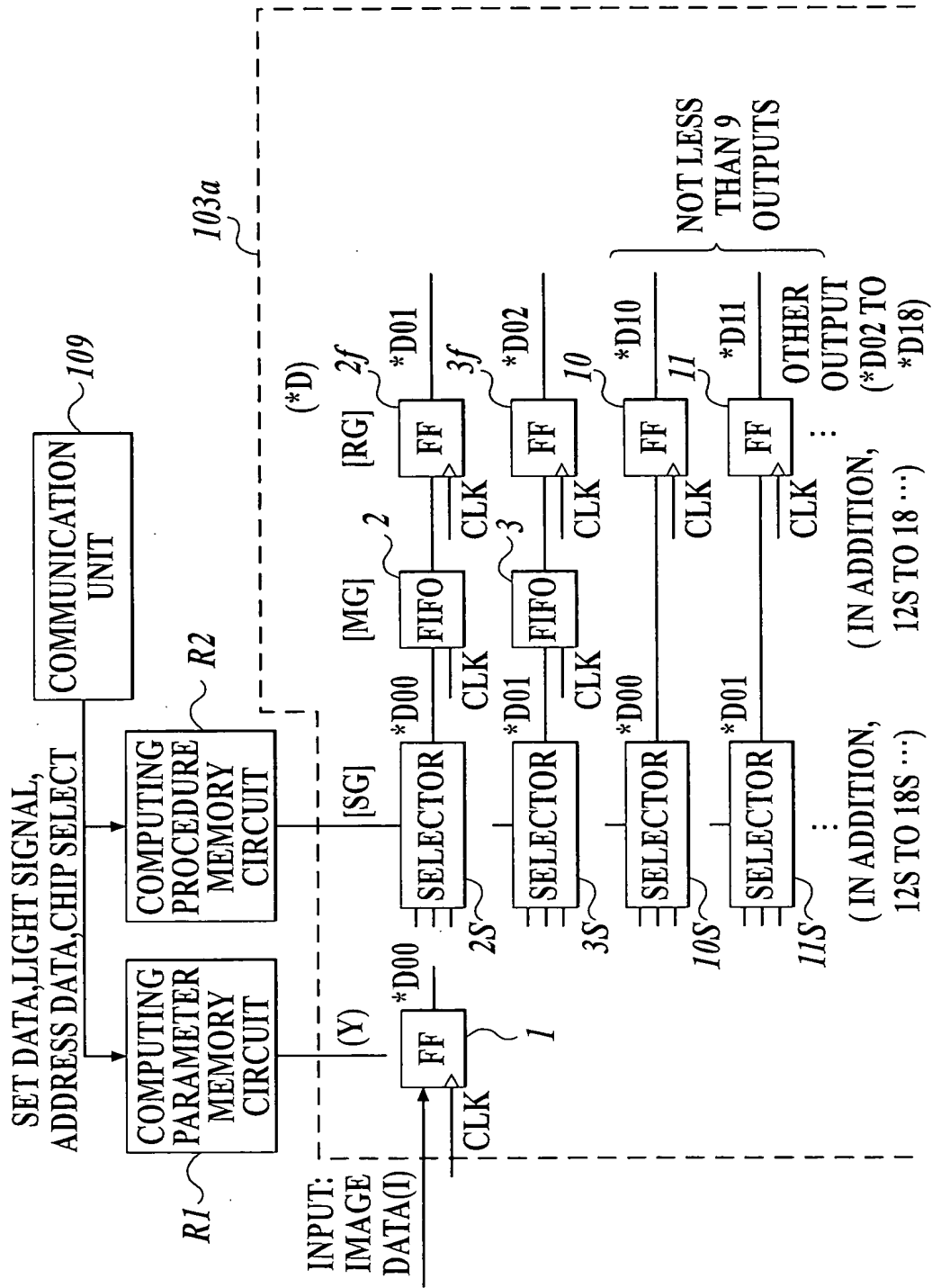


FIG. 3C

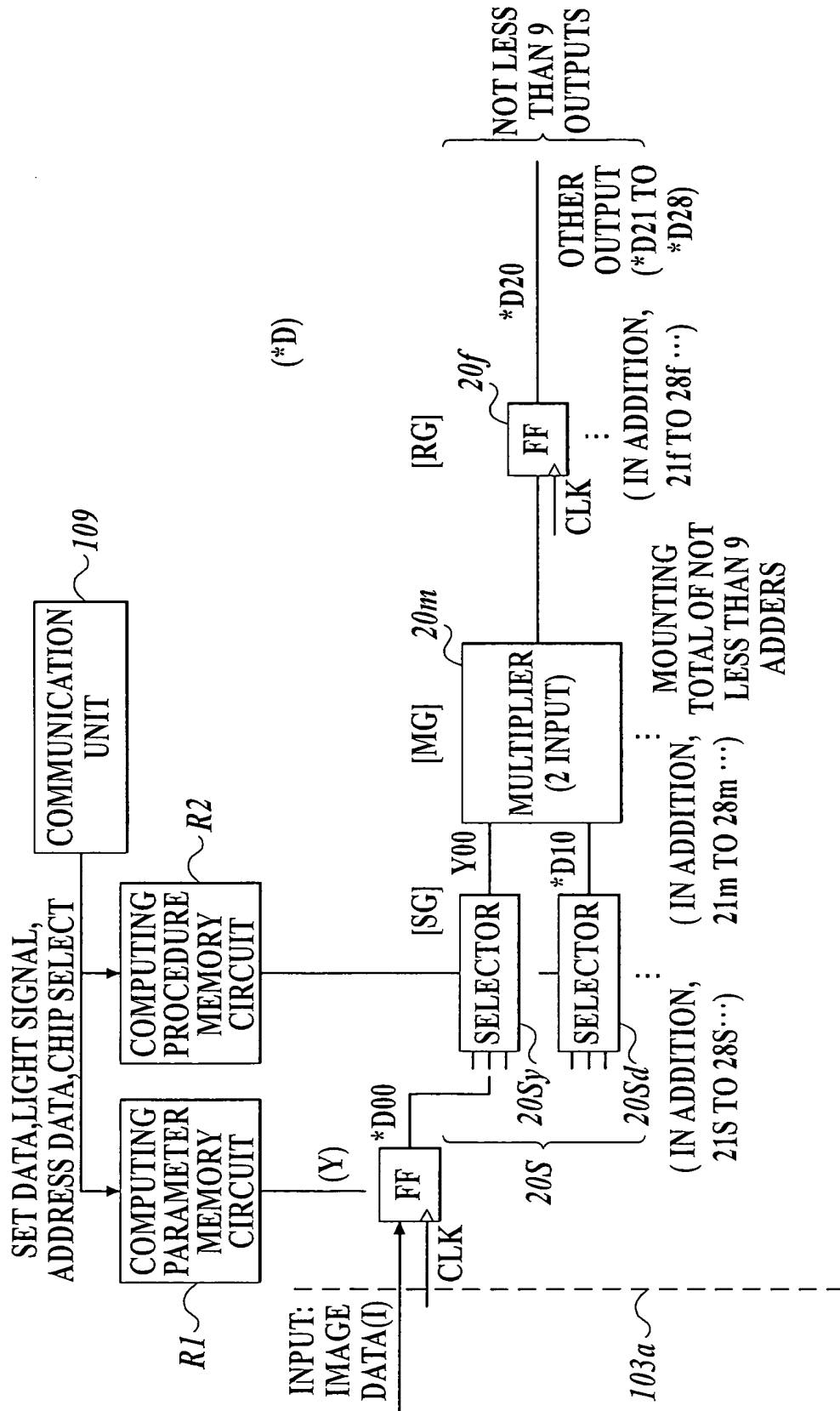


FIG.3D

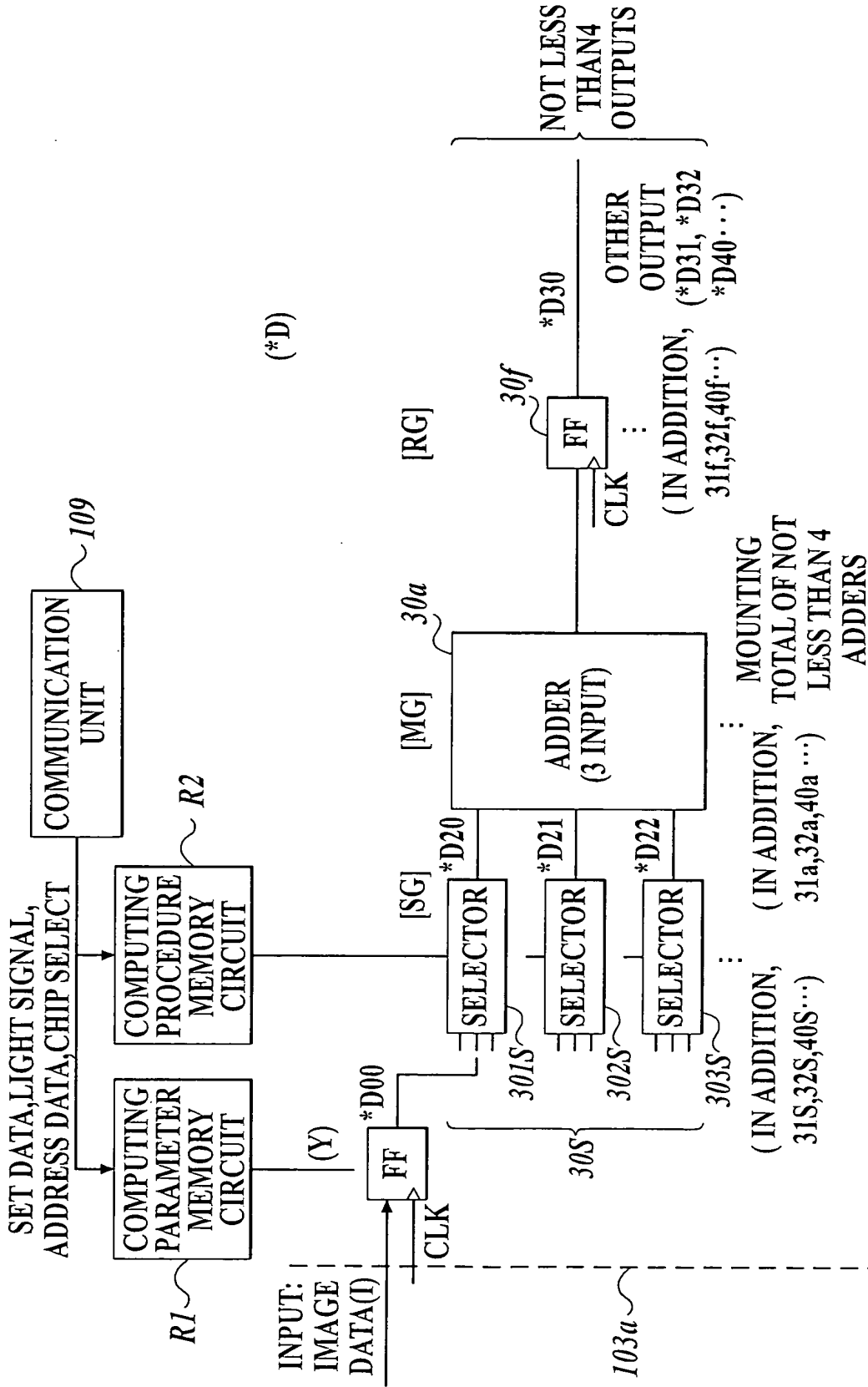


FIG. 3E

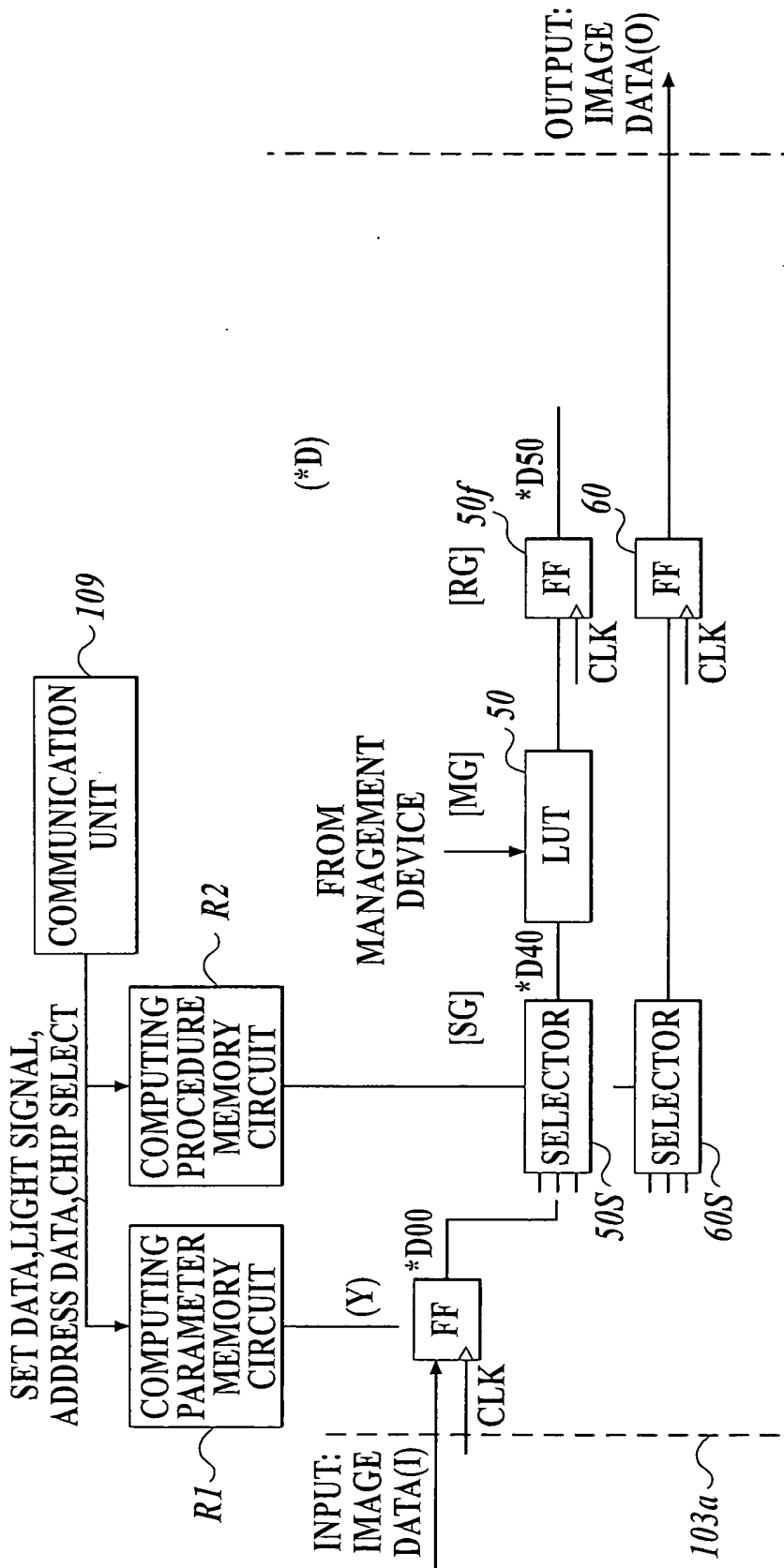


FIG.4A



FIG.4B



FIG.4C

LIGHT SIGNAL  
(NEGATIVE LOGIC)



INPUT IMAGE DATA



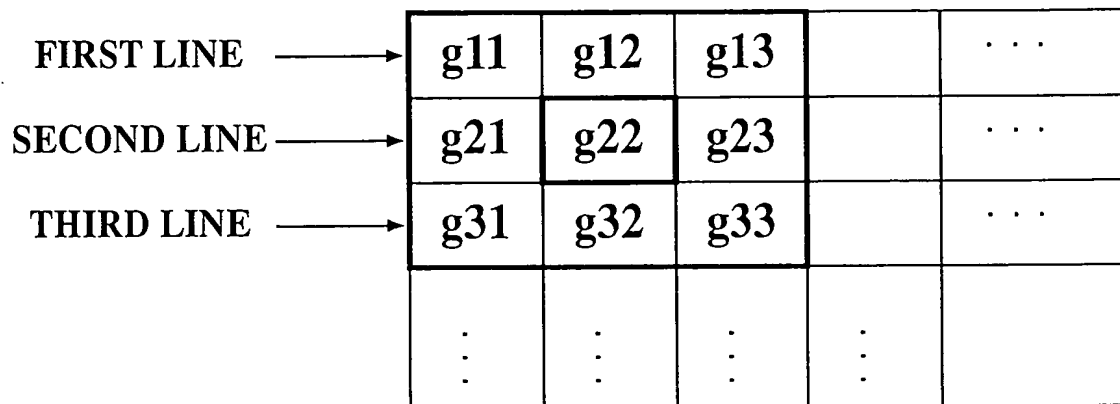
CLK





## IMAGE DATA

## MAIN SCANNING DIRECTION



**NOTE PIXEL g22**

FIG.6

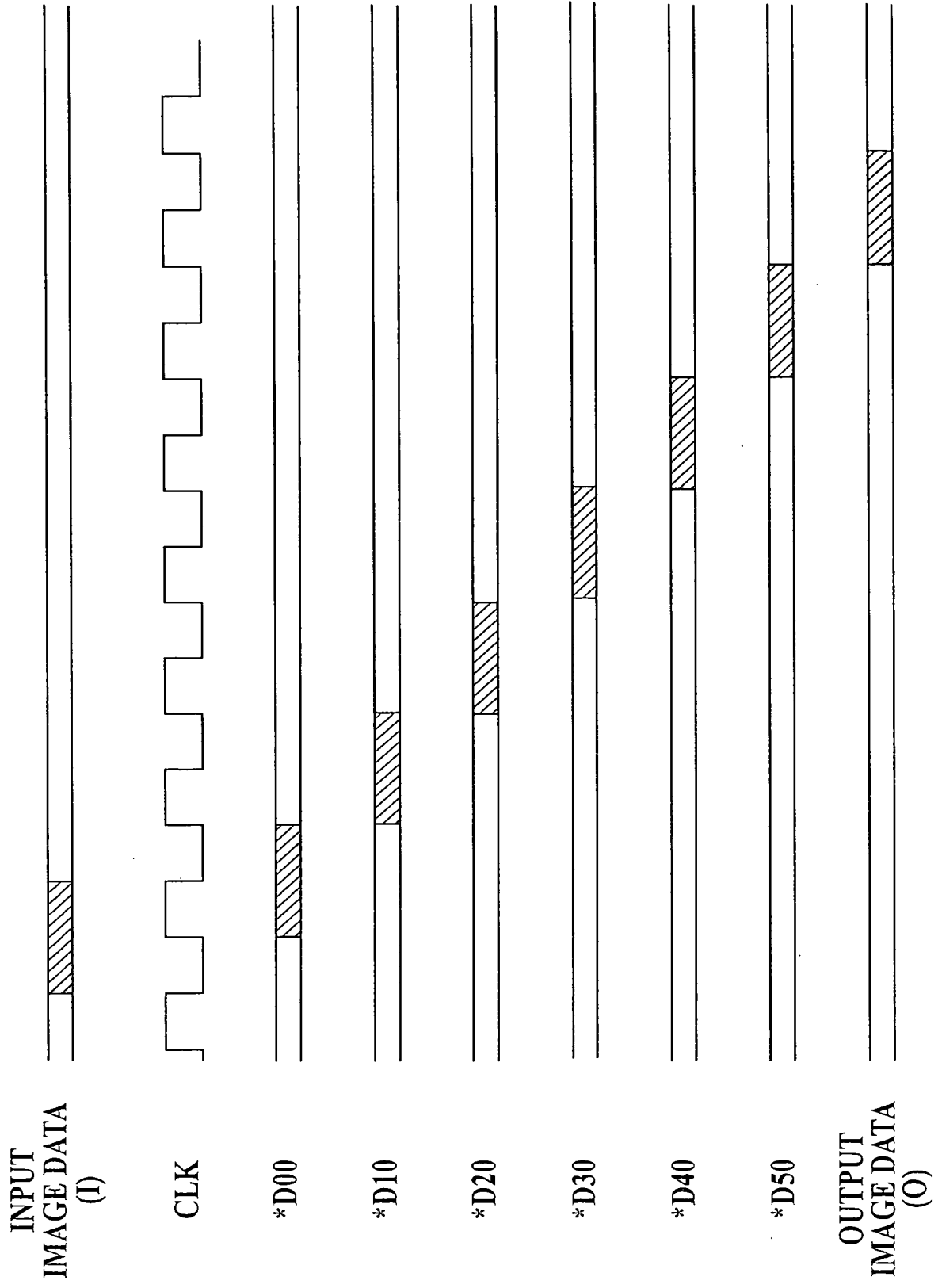
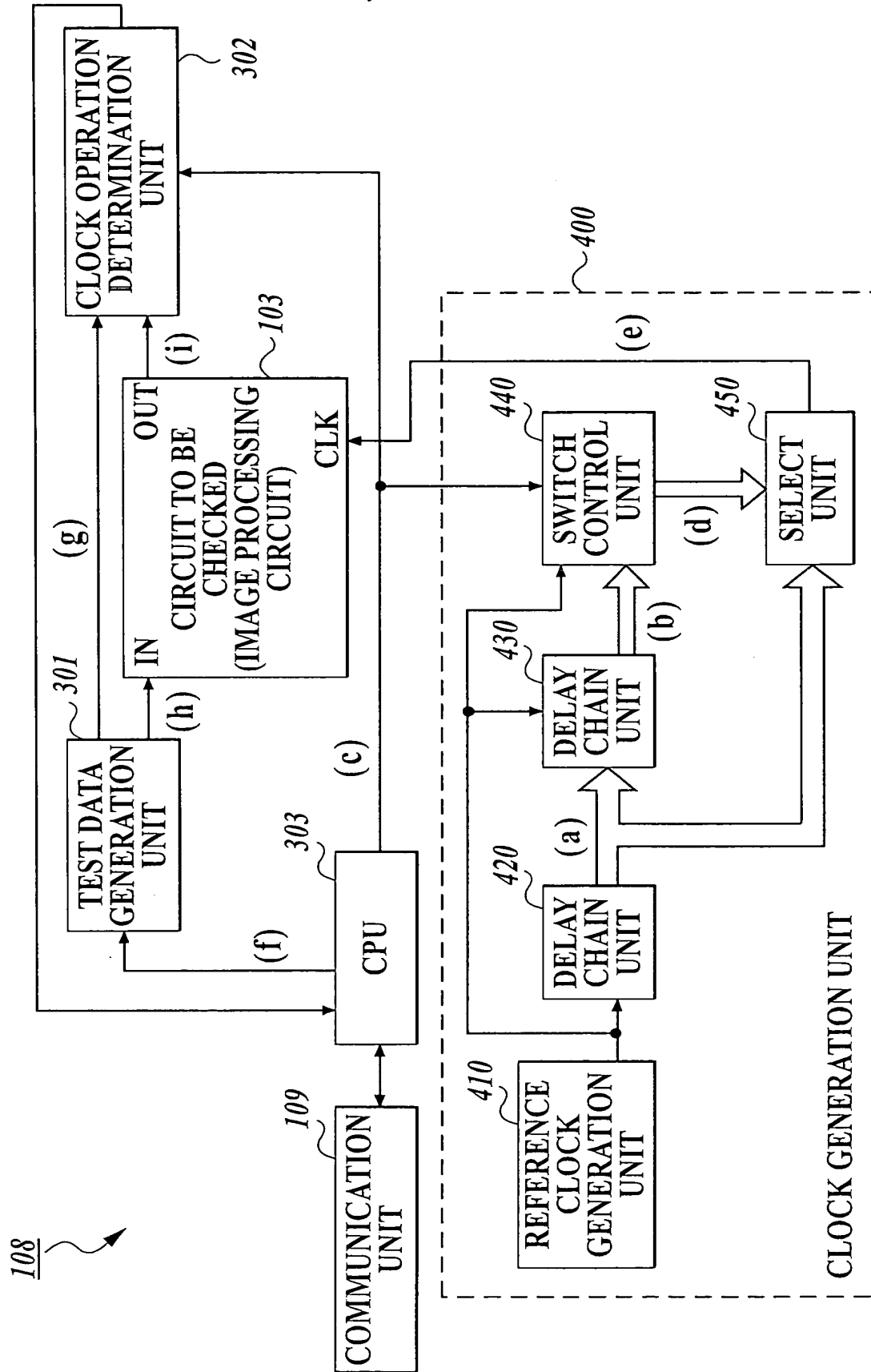


FIG. 7



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**FIG.8A**  
REFERENCE  
CLOCK

**FIG.8B**  
DL19

**FIG.8C**  
DL20

**FIG.8D**  
DL21

**FIG.8E**  
DL22

**FIG.8F**  
DL23

**FIG.8G**  
DL24

**FIG.8H**  
DL25

**FIG.8I**  
DL46

**FIG.8J**  
DL47

**FIG.8K**  
DL48

**FIG.8L**  
DL49

**FIG.8M**  
DL50

**FIG.8N**  
DL51

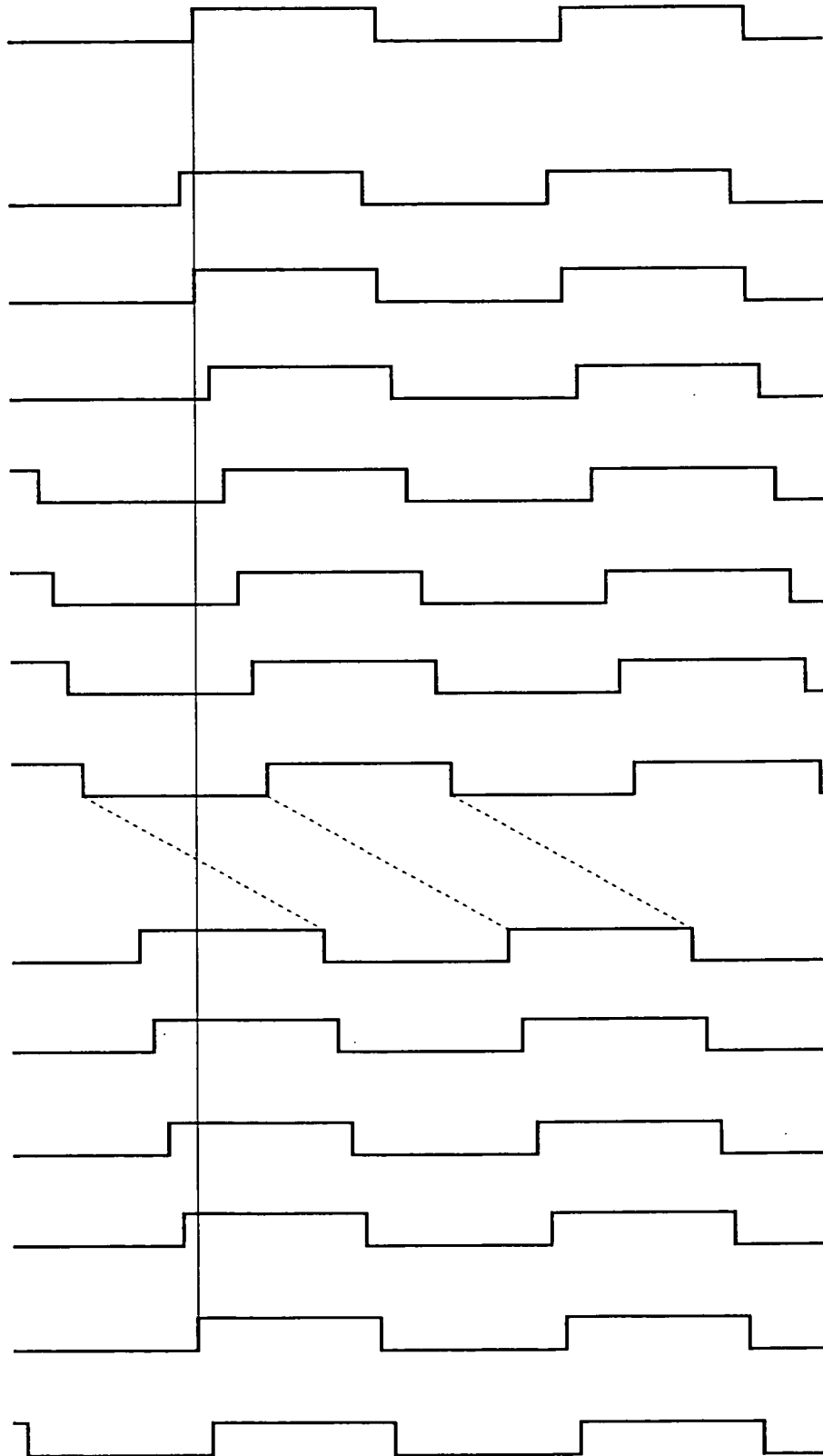


FIG.9

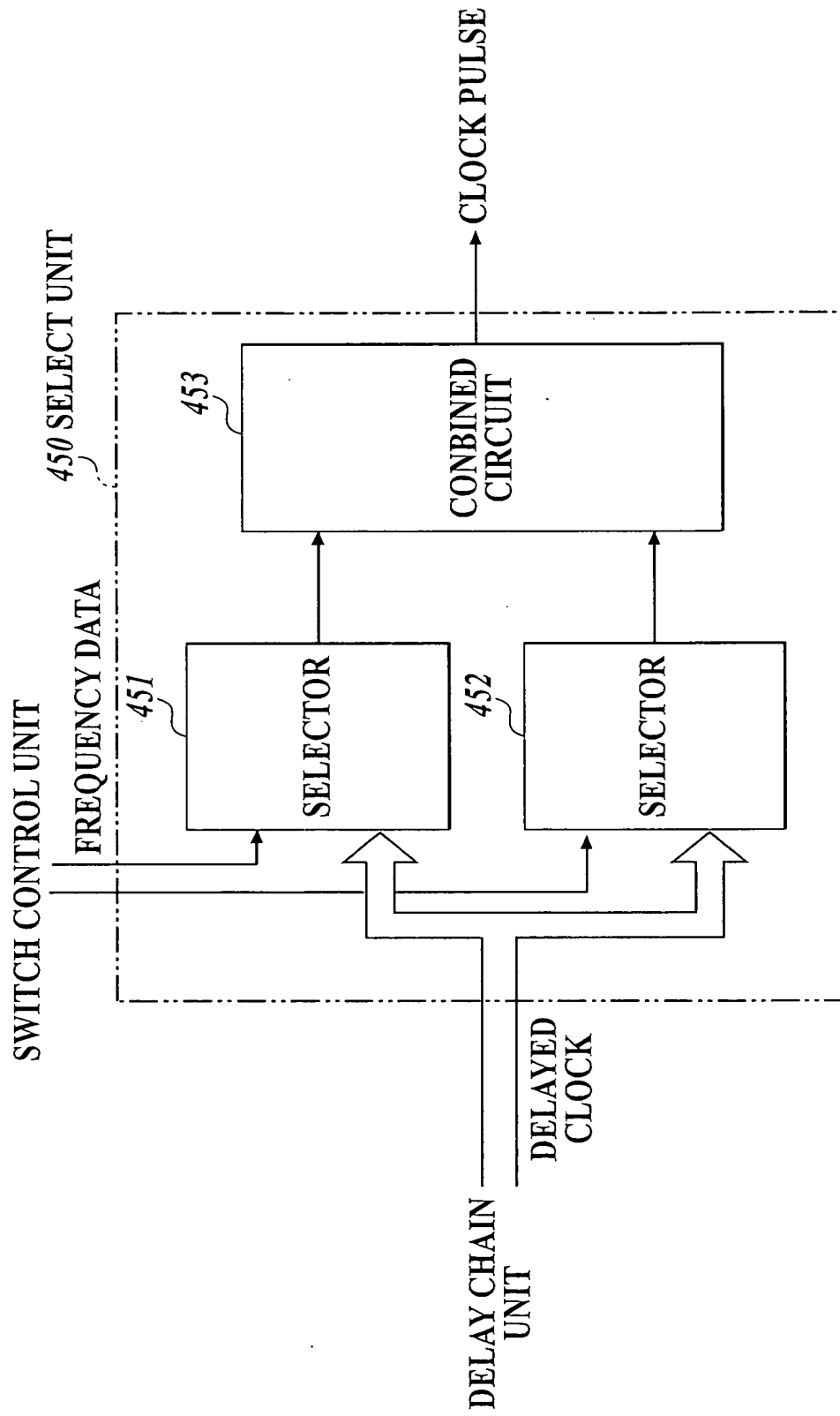


FIG.10A

REFERENCE CLOCK

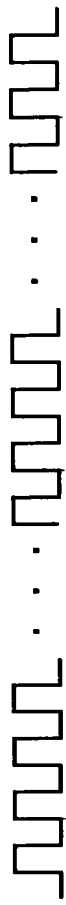


FIG.10B

START SIGNAL

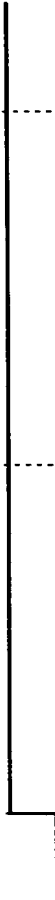


FIG.10C

FREQUENCY DATA



FIG.10D

CLOCK PULSE



FIG.10E

SET VALUE OF CIRCUIT TO BE CHECKED

*SET IN THE FIRST PLACE	*SET IN THE FIRST PLACE
-------------------------	-------------------------

FIG.10F

INPUT TEST DATA

00	01	.	.	.	00	01	.	.	.	20	.	.	.	.	00	01
----	----	---	---	---	----	----	---	---	---	----	---	---	---	---	----	----

FIG.10G

EXPECTED VALUE TEST DATA

ff	46	.	.	.	ff	46	.	.	.	37	.	.	.	.	f4	46
----	----	---	---	---	----	----	---	---	---	----	---	---	---	---	----	----

FIG.10H

OUTPUT TEST DATA

ff	46	.	.	.	ff	46	.	.	.	35	.	.	.	.	f1	46
----	----	---	---	---	----	----	---	---	---	----	---	---	---	---	----	----

FIG.10I

COMPARISON RESULT OF EXPECTED  
VALUE AND OUTPUT VALUE

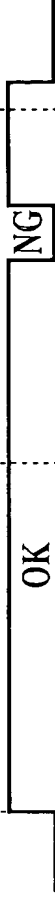
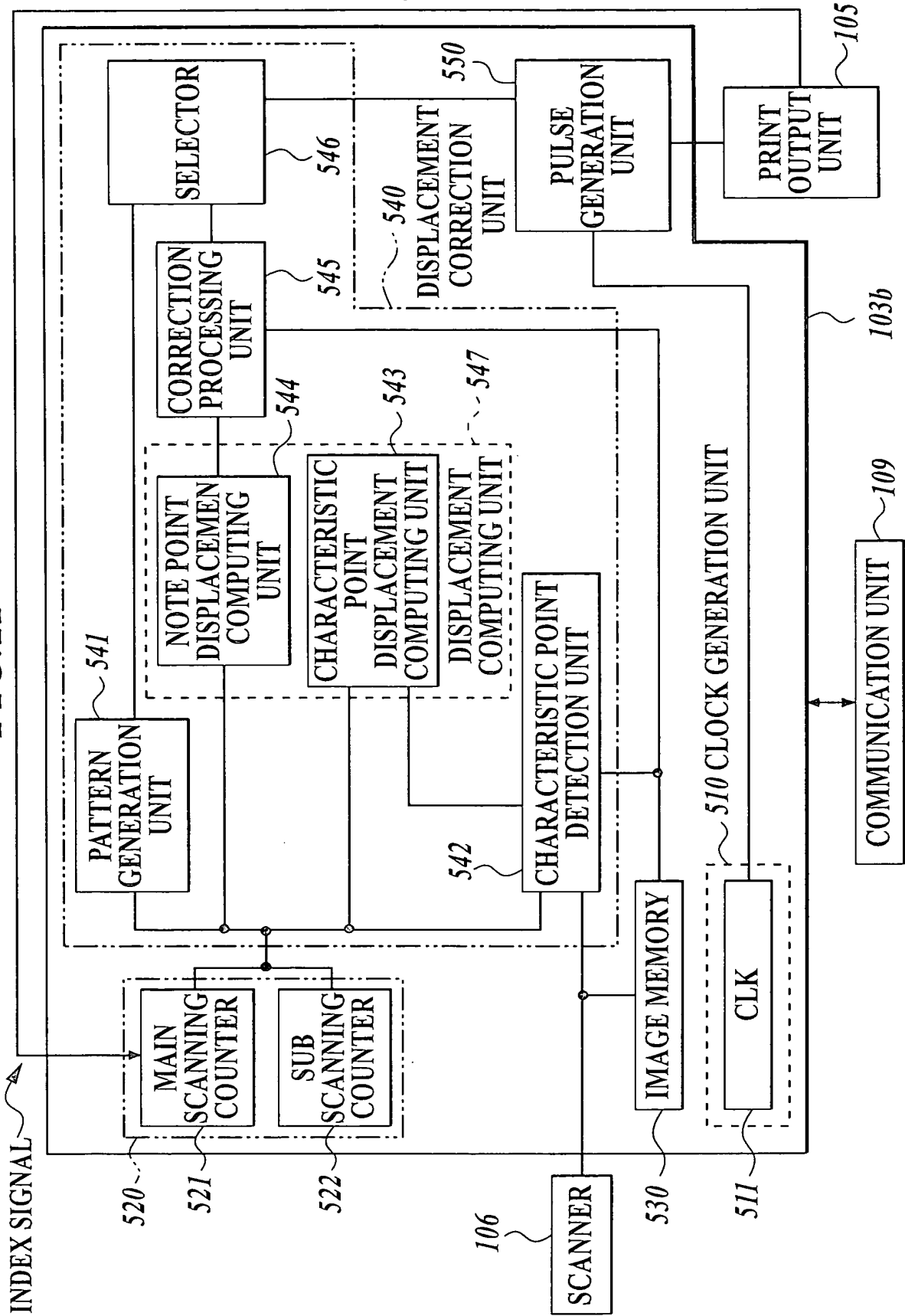


FIG.10J

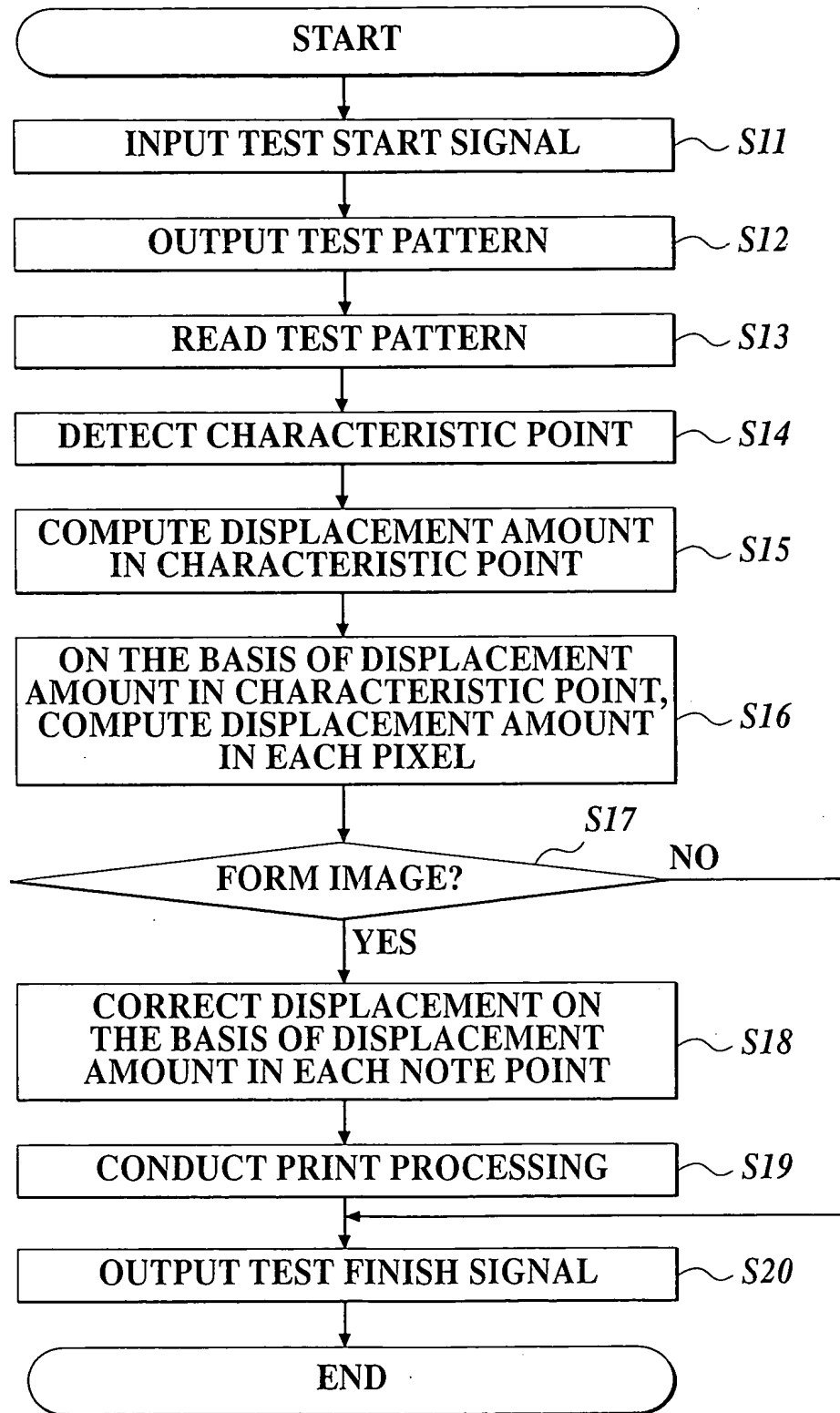
MAXIMUM OPERATION FREQUENCY

ON MEASURING	50MHz
--------------	-------

FIG. 11

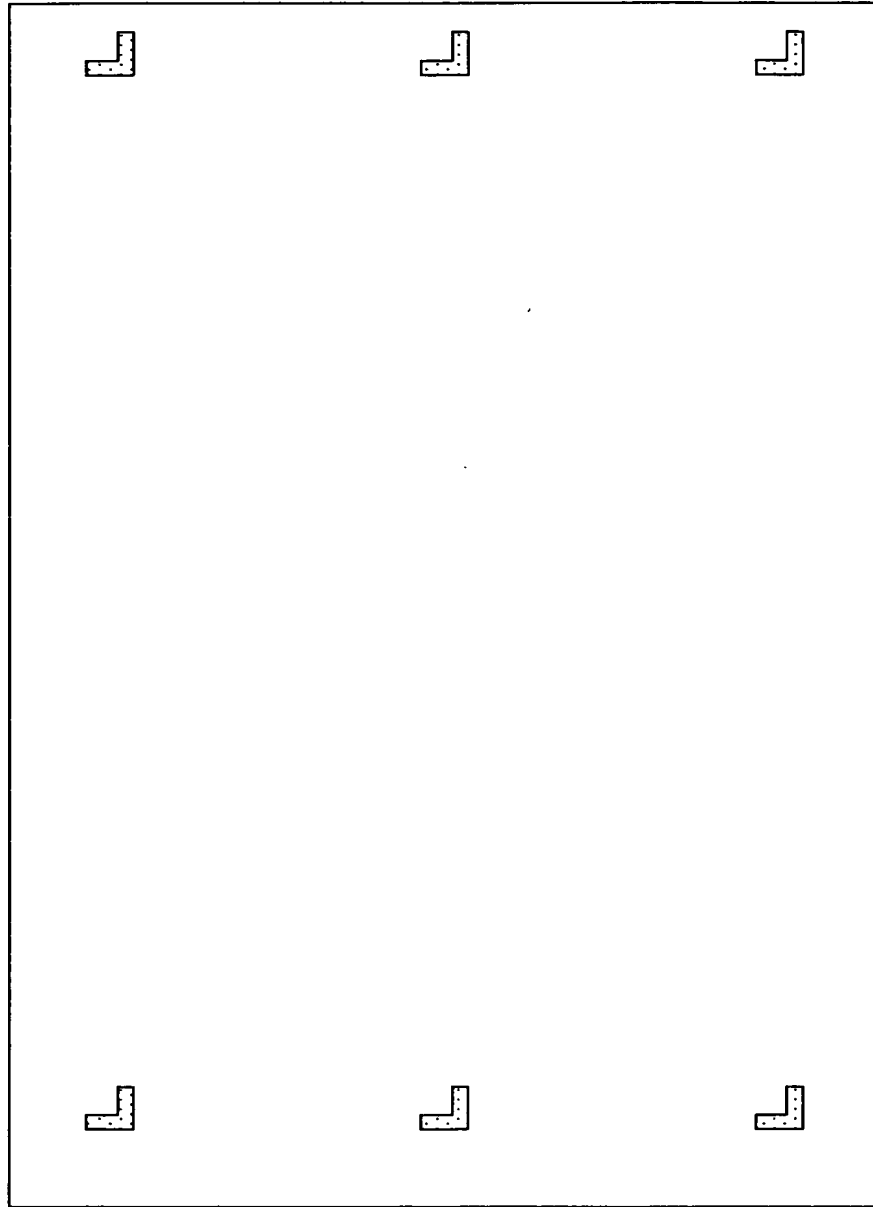


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**FIG.12**



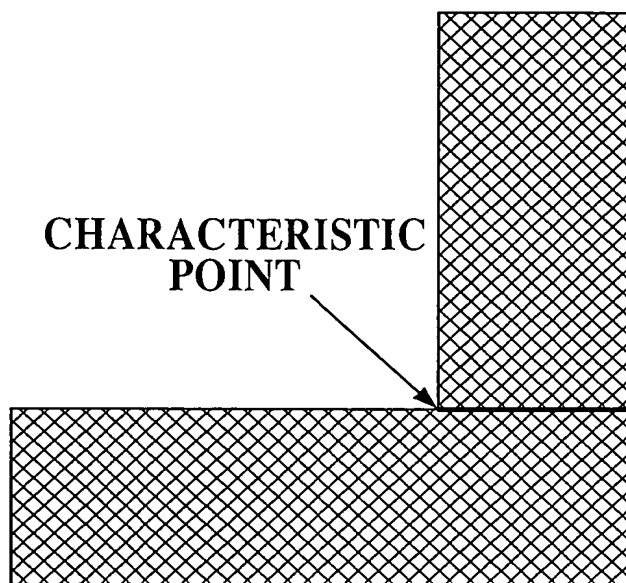


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***FIG.13***



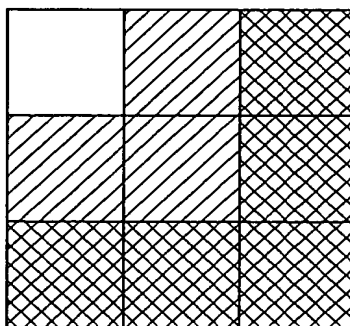
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**FIG.14A**



**FIG.14B**

MAIN SCANNING DIRECTION

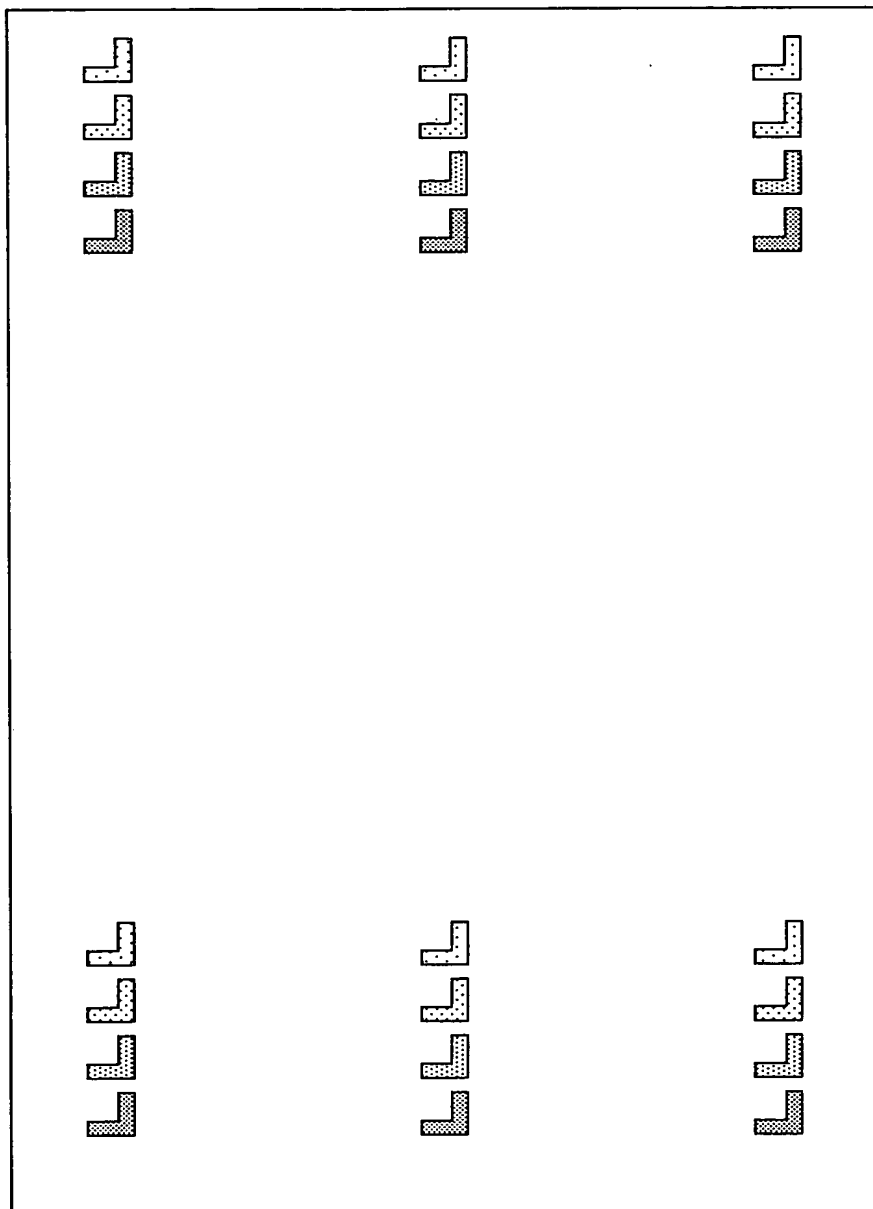


 : ZERO DENSITY(WHITE)

 : HALFTONE DENSITY

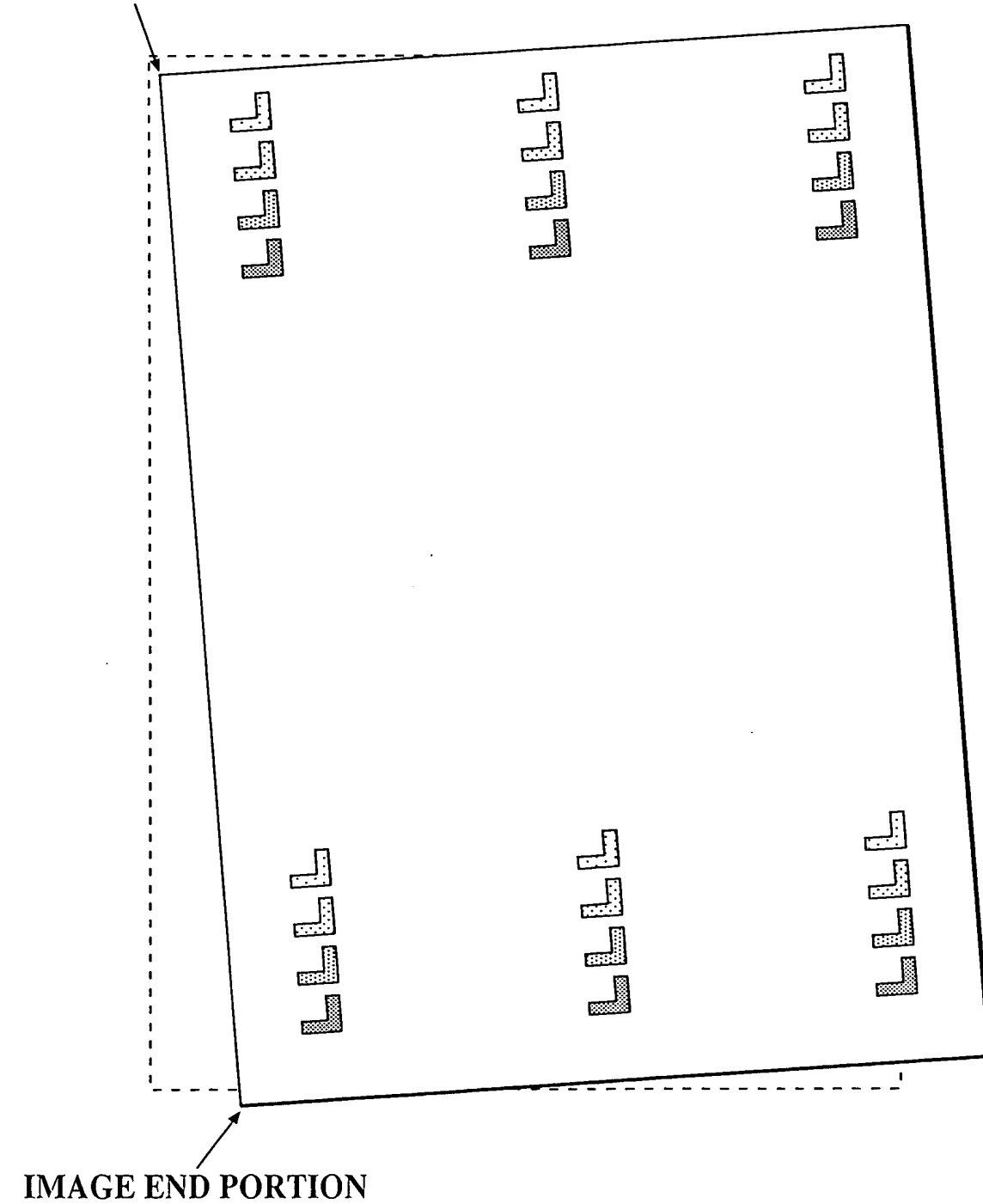
 : FULL DENSITY(BLACK)

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**FIG.15**



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**FIG.16**

IMAGE END PORTION



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**FIG.17**

